

ABSTRACT OF THE DISCLOSURE

Provided is a frequency multiplier including a delay circuit, an XOR gate, and a control circuit and a method of operating such a frequency multiplier to adjust the duty cycle of a clock signal. During operation of the frequency multiplier the delay circuit receives a first clock signal and generates a delayed clock signal. The XOR gate receives the first clock signal and the delayed clock signal, performs an XOR operation on the received signals and outputs a second clock signal that has a frequency that is a multiple of the first clock signal. The control circuit monitors the phase difference between the first clock signal and the delayed clock signal and outputs a control signal corresponding to the detected phase difference to the delay circuit to adjust the time delay applied to the first clock signal by the delay circuit.